

## CLAIMS

1. A electronically erasable read only memory, comprising:
  - a capacitor comprising:
    - a diffusion layer of a first conductivity type formed in a well of a second conductivity type;
    - an insulating layer overlying the diffusion layer; and
    - a floating gate overlying the diffusion layer; and
  - a MOS transistor comprising:
    - first and second active regions formed in the well, adjacent to an extended portion of the floating gate.
2. The electronically erasable read only memory of claim 1 wherein the first conductivity type is a p type and the second conductivity type is an n type.
3. The electronically erasable read only memory of claim 1 wherein the first conductivity type is an n type and the second conductivity type is a p type.
4. The electronically erasable read only memory of claim 1 and further comprising a second diffusion layer beneath one of the first and second active regions.
5. The electronically erasable read only memory of claim 4 wherein the first active regions comprises a source, the second active region comprises a drain, and the extended portion the floating gate comprises a gate of a MOS transistor, and the second diffusion layer is formed beneath the second active region.
6. A method of forming an electronically erasable read only memory, comprising the steps of:

forming a diffusion layer of a first conductivity type formed in a well of a second conductivity type;

- formulating an insulating layer overlying the diffusion layer; and
- formulating a floating gate overlying the diffusion layer; and
- 5 forming first and second active regions formed in the well, adjacent to an extended portion of the floating gate.

7. The method of claim 6 wherein the step of forming a diffusion layer comprises the step of forming a diffusion layer of a p conductivity type in a well of an n conductivity type.

- 10 8. The method of claim 6 wherein the step of forming a diffusion layer comprises the step of forming a diffusion layer of an n conductivity type in a well of a p conductivity type.

9. The method of claim 6 and further comprising the step of forming a second diffusion layer beneath one of the first and second active regions.

- 15 10. The method of claim 9 wherein the first active region comprises a source, the second active region comprises a drain, and the extended portion of the floating gate comprises a gate of a MOS transistor, and wherein the step of forming a second diffusion layer comprises the step of forming the second diffusion layer beneath the second active region.